

MJD18002D2

Bipolar NPN Transistor

High Speed, High Gain Bipolar NPN Power Transistor with Integrated Collector–Emitter Diode and Built–In Efficient Antisaturation Network

The MJD18002D2 is a state-of-the-art high speed, high gain bipolar transistor (H2BIP). Tight dynamic characteristics and lot to lot minimum spread (± 150 ns on storage time) make it ideally suitable for light ballast applications. Therefore, there is no longer a need to guarantee an h_{FE} window.

Main Features:

- Low Base Drive Requirement
- High Peak DC Current Gain (55 Typical) @ $I_C = 100$ mA
- **Extremely Low Storage Time Min/Max Guarantees Due to the H2BIP Structure which Minimizes the Spread**
- Integrated Collector–Emitter Free Wheeling Diode
- Fully Characterized and Guaranteed Dynamic V_{CEsat}
- Characteristics Make It Suitable for PFC Application
- “6 Sigma” Process Providing Tight and Reproducible Parameter Spreads

Two Versions:

- MJD18002D2–1: Case 369 for Insertion Mode
- MJD18002D2: Case 369A for Surface Mount Mode

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Sustaining Voltage	V_{CEO}	450	Vdc
Collector–Base Breakdown Voltage	V_{CBO}	1000	Vdc
Collector–Emitter Breakdown Voltage	V_{CES}	1000	Vdc
Emitter–Base Voltage	V_{EBO}	11	Vdc
Collector Current – Continuous – Peak (Note 1.)	I_C I_{CM}	2.0 5.0	Adc
Base Current – Continuous – Peak (Note 1.)	I_B I_{BM}	1.0 2.0	Adc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	50 0.4	W W/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	–65 to +150	$^\circ\text{C}$
Thermal Resistance – Junction–to–Case	$R_{\theta JC}$	5.0	$^\circ\text{C}/\text{W}$
Thermal Resistance – Junction–to–Ambient	$R_{\theta JA}$	71.4	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 sec.	T_L	260	$^\circ\text{C}$

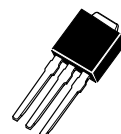
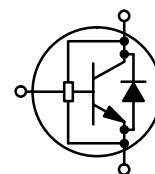
1. Pulse Test: Pulse Width = 5.0 ms, Duty Cycle = 10%



ON Semiconductor™

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**2 AMPERES
1000 VOLTS
50 WATTS
POWER TRANSISTOR**

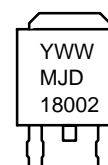
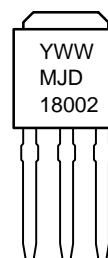


DPAK
CASE 369
STYLE 1



DPAK
CASE 369A
STYLE 1

MARKING DIAGRAMS



Y = Year
WW = Work Week
MJD18002 = Device Code

ORDERING INFORMATION

Device	Package	Shipping
MJD18002D2–1	DPAK	75 Units/Rail
MJD18002D2T4	DPAK	3000/Tape & Reel

MJD18002D2

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage ($I_C = 100\text{ mA}$, $L = 25\text{ mH}$)	$V_{CEO(sus)}$	450	570	–	Vdc
Collector–Base Breakdown Voltage ($I_{CBO} = 1\text{ mA}$)	V_{CBO}	1000	1100	–	Vdc
Emitter–Base Breakdown Voltage ($I_{EBO} = 1\text{ mA}$)	V_{EBO}	11	14	–	Vdc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CEO}$, $I_B = 0$)	I_{CEO}	–	–	100	μA dc
Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CES}$, $V_{EB} = 0$) ($V_{CE} = 500\text{ V}$, $V_{EB} = 0$)	@ $T_C = 25^\circ\text{C}$	–	–	100	μA dc
	@ $T_C = 125^\circ\text{C}$	–	–	500	
	@ $T_C = 125^\circ\text{C}$	–	–	100	
Emitter–Cutoff Current ($V_{EB} = 10\text{ Vdc}$, $I_C = 0$)	I_{EBO}	–	–	500	μA dc

ON CHARACTERISTICS

Base–Emitter Saturation Voltage ($I_C = 0.4\text{ Adc}$, $I_B = 40\text{ mA}$ dc) ($I_C = 1.0\text{ Adc}$, $I_B = 0.2\text{ Adc}$)	@ $T_C = 25^\circ\text{C}$	$V_{BE(sat)}$	–	0.78	1.0	Vdc
	@ $T_C = 125^\circ\text{C}$		–	0.87	1.1	
Collector–Emitter Saturation Voltage ($I_C = 0.4\text{ Adc}$, $I_B = 40\text{ mA}$ dc) ($I_C = 1.0\text{ Adc}$, $I_B = 0.2\text{ Adc}$)	@ $T_C = 25^\circ\text{C}$	$V_{CE(sat)}$	–	0.36	0.6	Vdc
	@ $T_C = 125^\circ\text{C}$		–	0.50	1.0	
	@ $T_C = 25^\circ\text{C}$		–	0.40	0.75	
	@ $T_C = 125^\circ\text{C}$		–	0.65	1.2	
DC Current Gain ($I_C = 0.4\text{ Adc}$, $V_{CE} = 1.0\text{ Vdc}$) ($I_C = 1.0\text{ Adc}$, $V_{CE} = 1.0\text{ Vdc}$)	@ $T_C = 25^\circ\text{C}$	h_{FE}	14	25	–	–
	@ $T_C = 125^\circ\text{C}$		8.0	15	–	
	@ $T_C = 25^\circ\text{C}$		6.0	10	–	
	@ $T_C = 125^\circ\text{C}$		4.0	6.0	–	

DYNAMIC CHARACTERISTICS

Current Gain Bandwidth ($I_C = 0.5\text{ Adc}$, $V_{CE} = 10\text{ Vdc}$, $f = 1\text{ MHz}$)	f_t	–	13	–	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 1\text{ MHz}$)	C_{ob}	–	50	100	pF
Input Capacitance ($V_{EB} = 8\text{ Vdc}$)	C_{ib}	–	340	500	pF

DIODE CHARACTERISTICS

Forward Diode Voltage ($I_{EC} = 1.0\text{ Adc}$) ($I_{EC} = 0.4\text{ Adc}$)	@ $T_C = 25^\circ\text{C}$	V_{EC}	–	1.2	1.5	Vdc
	@ $T_C = 25^\circ\text{C}$		–	1.0	1.3	
	@ $T_C = 125^\circ\text{C}$		–	0.6	–	
Forward Recovery Time ($I_F = 0.4\text{ Adc}$, $di/dt = 10\text{ A}/\mu\text{s}$) ($I_F = 1.0\text{ Adc}$, $di/dt = 10\text{ A}/\mu\text{s}$)	@ $T_C = 25^\circ\text{C}$	t_{fr}	–	517	–	ns
	@ $T_C = 25^\circ\text{C}$		–	480	–	

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ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic				Symbol	Min	Typ	Max	Unit
DYNAMIC SATURATION VOLTAGE								
Dynamic Saturation Voltage Determined 1 μs and 3 μs respectively after rising I_{B1} reaches 90% of final I_{B1}	$I_C = 0.4 \text{ Adc}$ $I_{B1} = 40 \text{ mA}$ $V_{CC} = 300 \text{ Vdc}$	@ 1 μs	@ $T_C = 25^\circ\text{C}$	$V_{CE(dsat)}$	–	7.4	–	V
		@ 3 μs	@ $T_C = 25^\circ\text{C}$		–	2.5	–	
	$I_C = 1 \text{ Adc}$ $I_{B1} = 0.2 \text{ A}$ $V_{CC} = 300 \text{ Vdc}$	@ 1 μs	@ $T_C = 25^\circ\text{C}$		–	11.7	–	
		@ 3 μs	@ $T_C = 25^\circ\text{C}$		–	1.3	–	

SWITCHING CHARACTERISTICS: Resistive Load (D.C.S. 10%, Pulse Width = 40 μs)

Turn-on Time	$I_C = 0.4 \text{ Adc}, I_{B1} = 40 \text{ mAdc}$ $I_{B2} = 200 \text{ mAdc}$ $V_{CC} = 300 \text{ Vdc}$	@ $T_C = 25^\circ\text{C}$	t_{on}	–	225	350	ns
Turn-off Time		@ $T_C = 125^\circ\text{C}$	t_{off}	0.8	–	1.1	μs
Turn-on Time	$I_C = 1.0 \text{ Adc}, I_{B1} = 0.2 \text{ Adc}$ $I_{B2} = 0.5 \text{ Adc}$ $V_{CC} = 300 \text{ Vdc}$	@ $T_C = 25^\circ\text{C}$	t_{on}	–	100	150	ns
Turn-off Time		@ $T_C = 125^\circ\text{C}$	t_{off}	0.95	–	1.25	μs

SWITCHING CHARACTERISTICS: Inductive Load ($V_{clamp} = 300 \text{ V}, V_{CC} = 15 \text{ V}, L = 200 \mu\text{H}$)

Fall Time	$I_C = 0.4 \text{ Adc}$ $I_{B1} = 40 \text{ mAdc}$ $I_{B2} = 0.2 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$	t_f	–	130	175	ns
Storage Time		@ $T_C = 125^\circ\text{C}$	t_s	0.4	–	0.7	μs
Cross-over Time		@ $T_C = 25^\circ\text{C}$	t_c	–	110	175	ns
		@ $T_C = 125^\circ\text{C}$		–	100	–	
Fall Time	$I_C = 0.8 \text{ Adc}$ $I_{B1} = 160 \text{ mAdc}$ $I_{B2} = 160 \text{ mAdc}$	@ $T_C = 25^\circ\text{C}$	t_f	–	130	175	ns
Storage Time		@ $T_C = 125^\circ\text{C}$	t_s	2.1	–	2.4	μs
Cross-over Time		@ $T_C = 25^\circ\text{C}$	t_c	–	275	350	ns
		@ $T_C = 125^\circ\text{C}$		–	350	–	
Fall Time	$I_C = 1.0 \text{ Adc}$ $I_{B1} = 0.2 \text{ Adc}$ $I_{B2} = 0.5 \text{ Adc}$	@ $T_C = 25^\circ\text{C}$	t_f	–	100	150	ns
Storage Time		@ $T_C = 125^\circ\text{C}$	t_s	–	1.05	1.2	μs
Cross-over Time		@ $T_C = 25^\circ\text{C}$	t_c	–	100	150	ns
		@ $T_C = 125^\circ\text{C}$		–	115	–	

Typical Static Characteristics

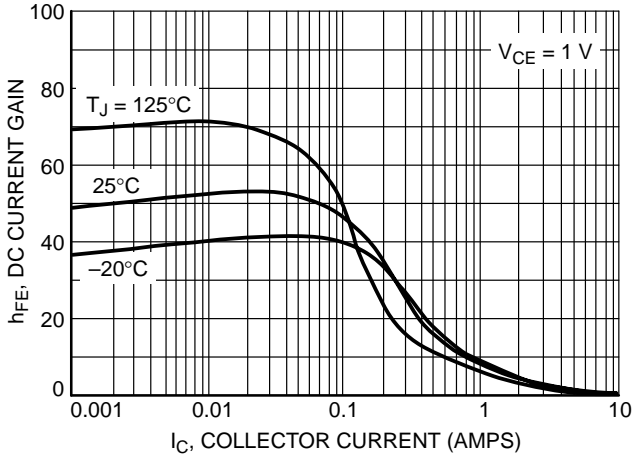


Figure 1. DC Current Gain @ 1 V

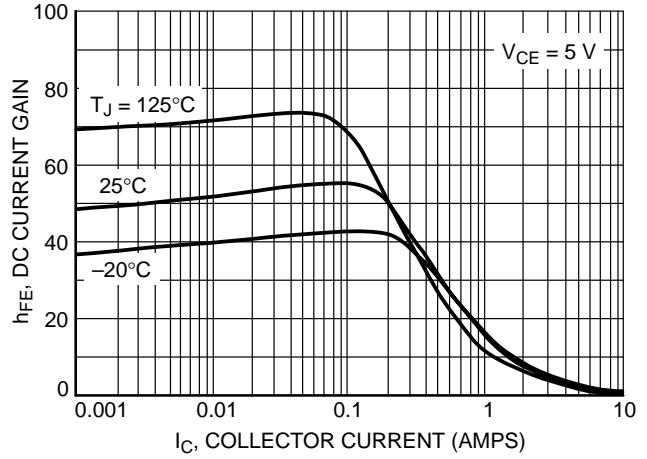


Figure 2. DC Current Gain @ 5 V

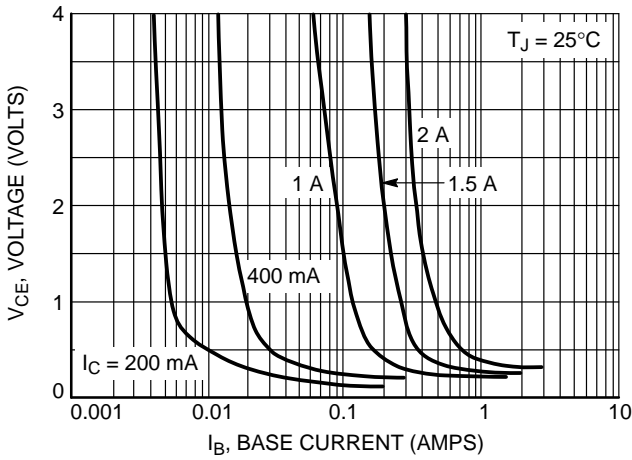


Figure 3. Collector Saturation Region

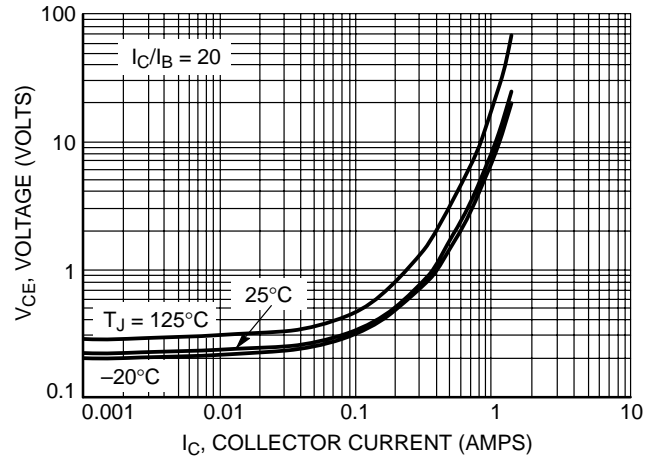


Figure 4. Collector-Emitter Saturation Voltage

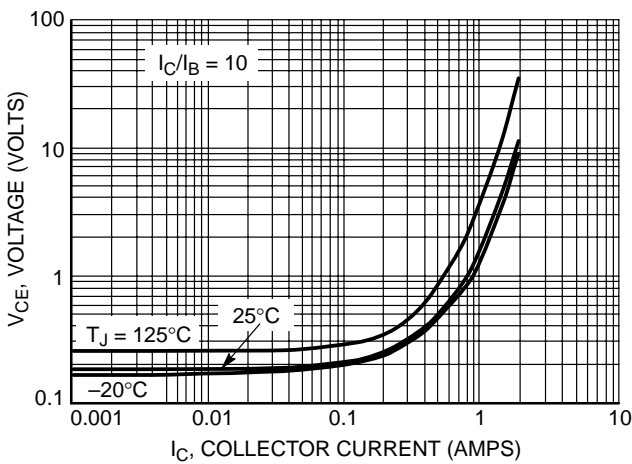


Figure 5. Collector-Emitter Saturation Voltage

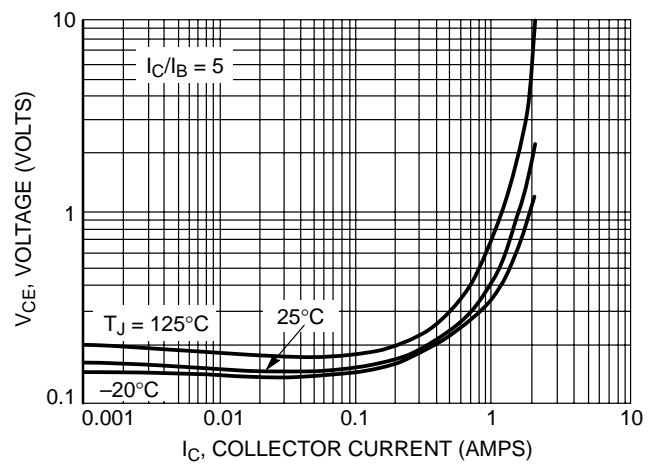


Figure 6. Collector-Emitter Saturation Voltage

Typical Static Characteristics

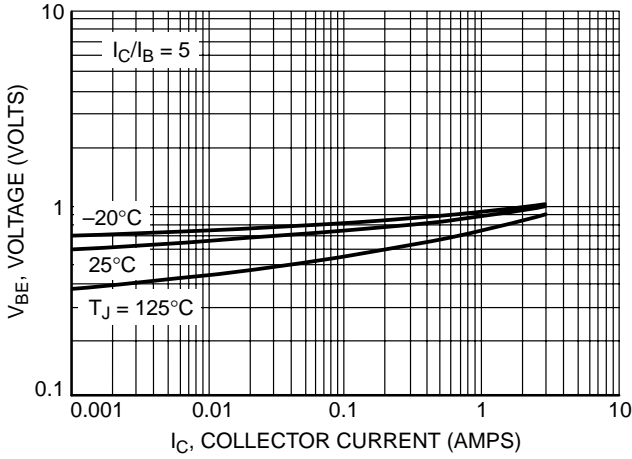


Figure 7. Base-Emitter Saturation Region
 $I_C/I_B = 5$

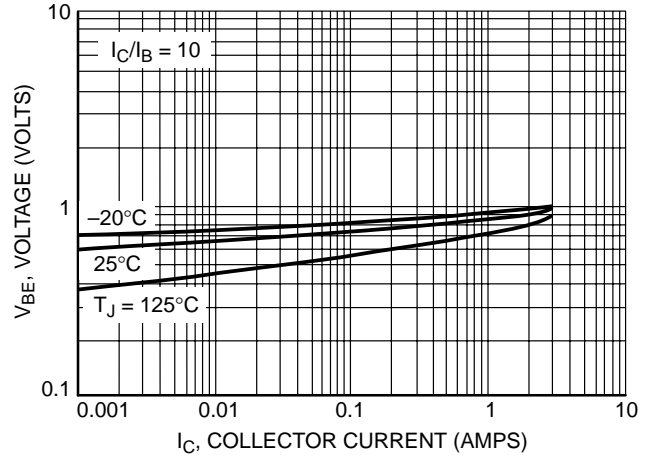


Figure 8. Base-Emitter Saturation Region
 $I_C/I_B = 10$

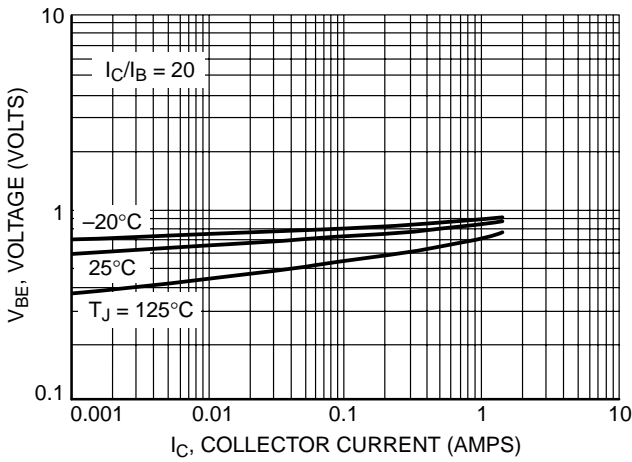


Figure 9. Base-Emitter Saturation Region
 $I_C/I_B = 20$

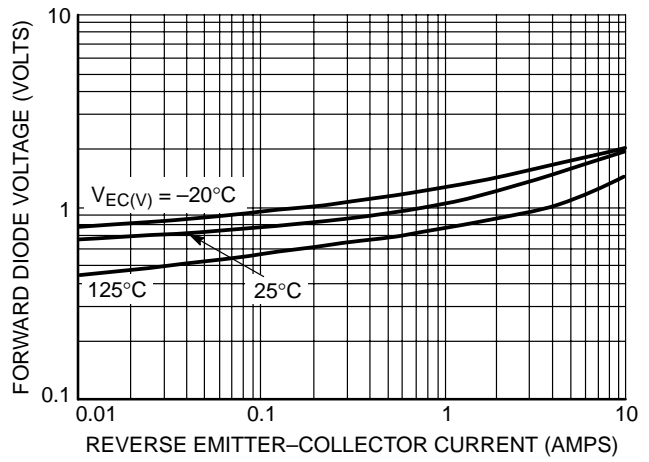


Figure 10. Forward Diode Voltage

Typical Switching Characteristics

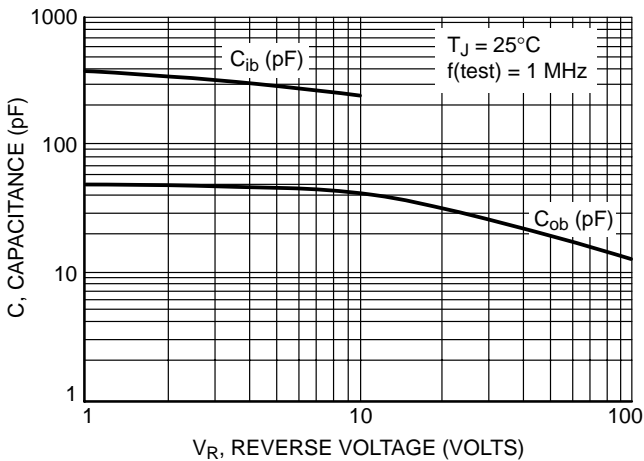


Figure 11. Capacitance

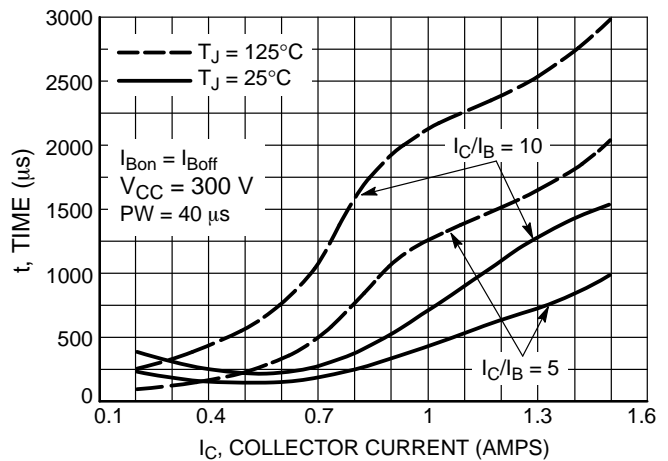


Figure 12. Resistive Switch Time, t_{on}

Typical Switching Characteristics

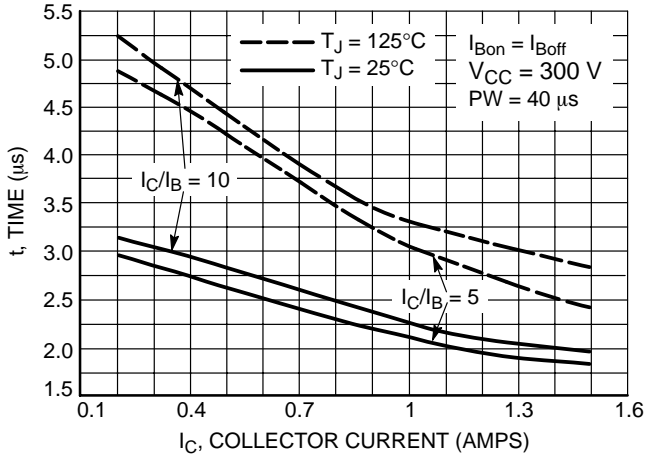


Figure 13. Resistive Switch Time, t_{off}

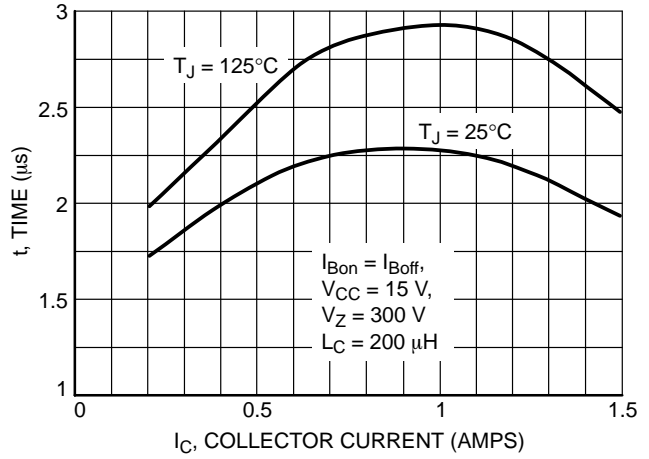


Figure 14. Inductive Storage Time, t_{si} @ $I_C/I_B = 5$

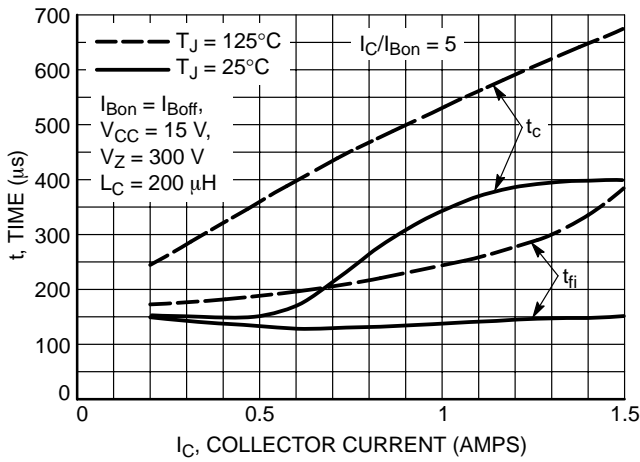


Figure 15. Inductive Switching, t_c & t_{fi} @ $I_C/I_B = 5$

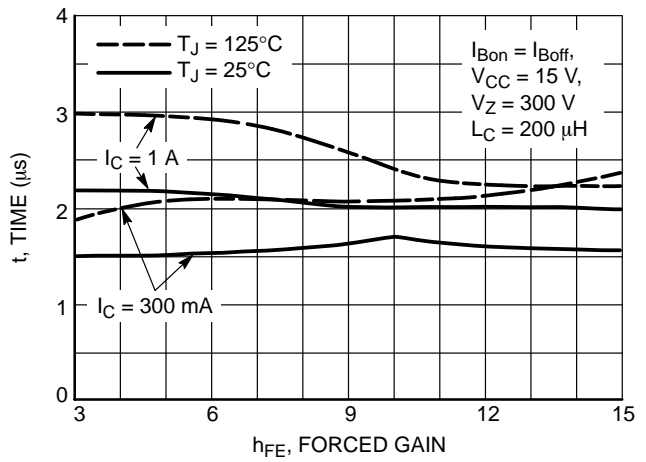


Figure 16. Inductive Storage Time

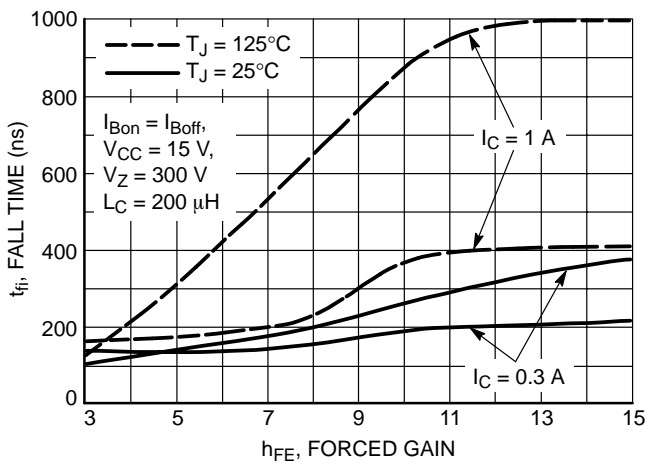


Figure 17. Inductive Fall Time

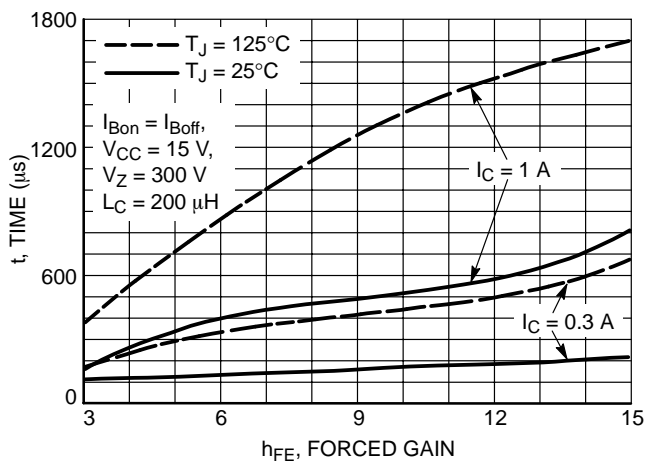


Figure 18. Inductive Cross-Over Time

Typical Switching Characteristics

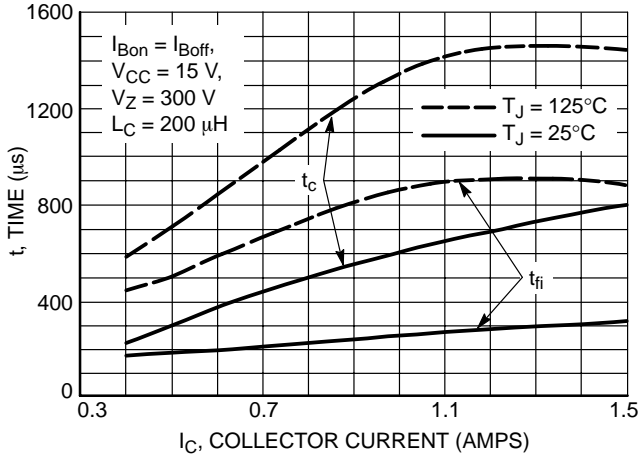


Figure 19. Inductive Switching Time, t_{fi} & T_C @ $G = 10$

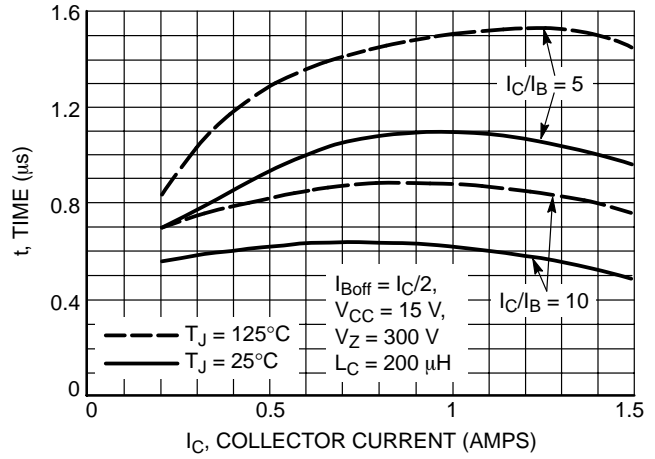


Figure 20. Inductive Switching Time, t_{si}

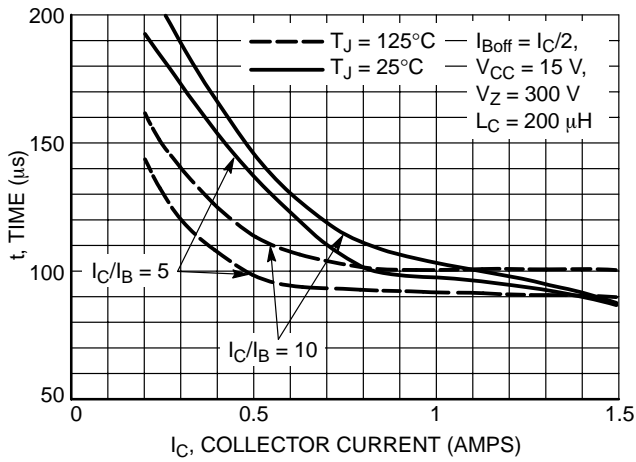


Figure 21. Inductive Storage Time, t_{fi}

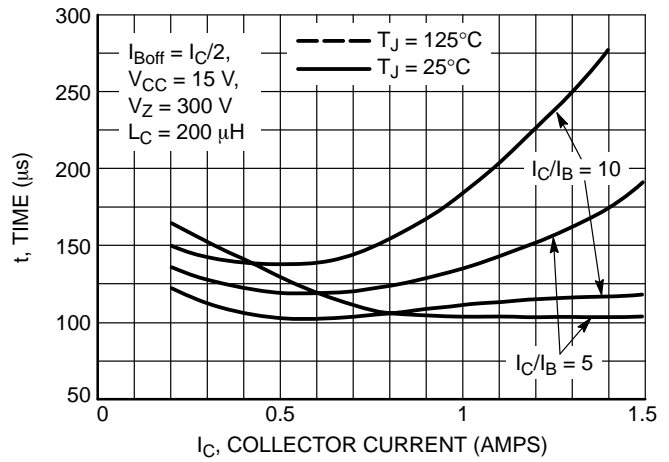


Figure 22. Inductive Storage Time, t_c

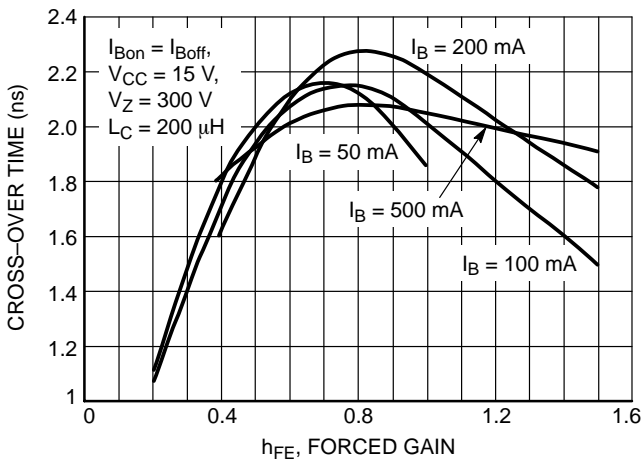


Figure 23. Inductive Storage Time, t_{si}

Figure 24. Dynamic Saturation Voltage Measurements

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Typical Switching Characteristics

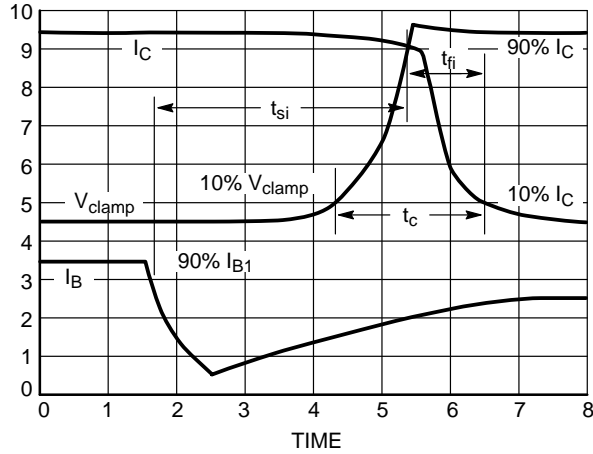
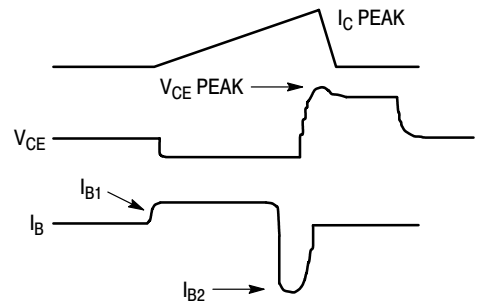
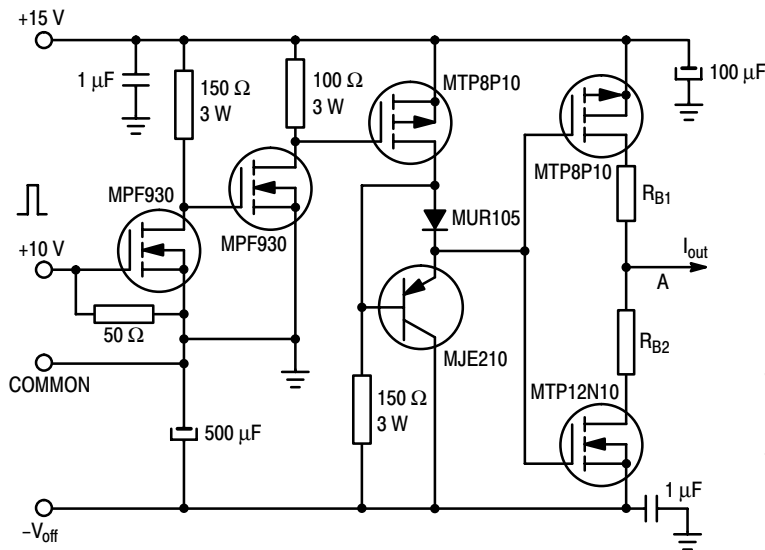


Figure 25. Inductive Switching Measurements

Table 1. Inductive Load Switching Drive Circuit



$V_{(BR)CEO(sus)}$
 $L = 10\text{ mH}$
 $R_{B2} = \infty$
 $V_{CC} = 20\text{ Volts}$
 $I_{C(pk)} = 100\text{ mA}$

Inductive Switching
 $L = 200\text{ }\mu\text{H}$
 $R_{B2} = 0$
 $V_{CC} = 15\text{ Volts}$
 R_{B1} selected for desired I_{B1}

RBSOA
 $L = 500\text{ }\mu\text{H}$
 $R_{B2} = 0$
 $V_{CC} = 15\text{ Volts}$
 R_{B1} selected for desired I_{B1}

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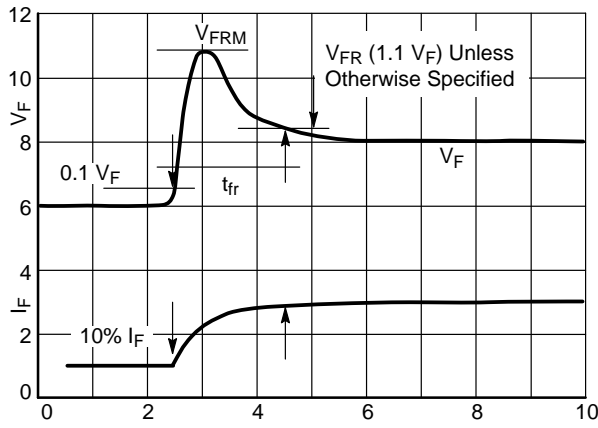


Figure 26. t_{fr} Measurement

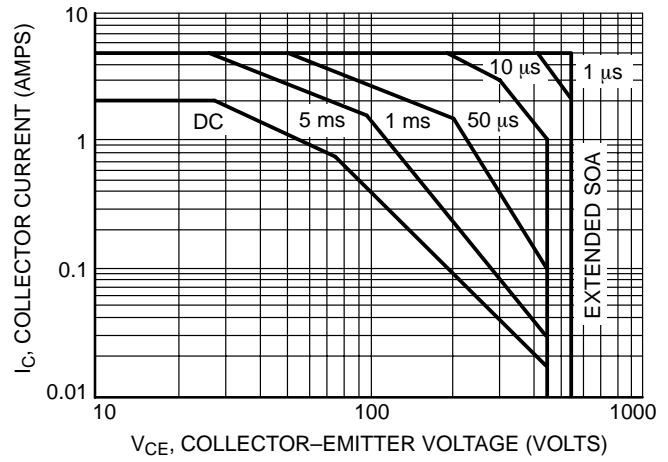


Figure 27. Forward Bias Safe Operating Area

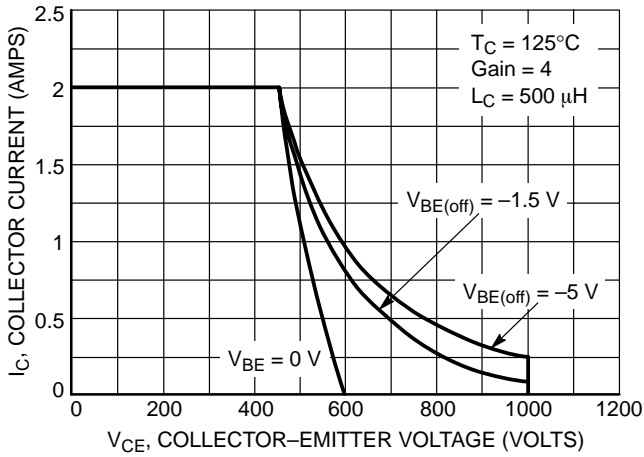


Figure 28. Reverse Bias Safe Operating Area

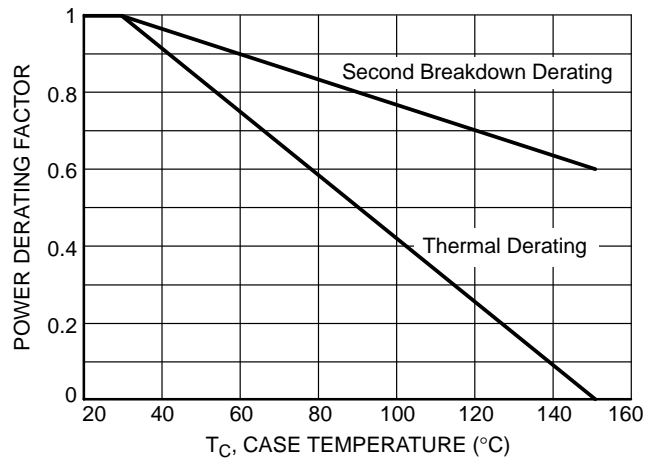


Figure 29. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 27 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C > 25^\circ\text{C}$. Second Breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on

Figure 27 may be found at any case temperature by using the appropriate curve on Figure 29.

$T_{J(pk)}$ may be calculated from the data in Figure 30. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base to emitter junction reverse biased. The safe level is specified as a reverse biased safe operating area (Figure 28). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

MJD18002D2

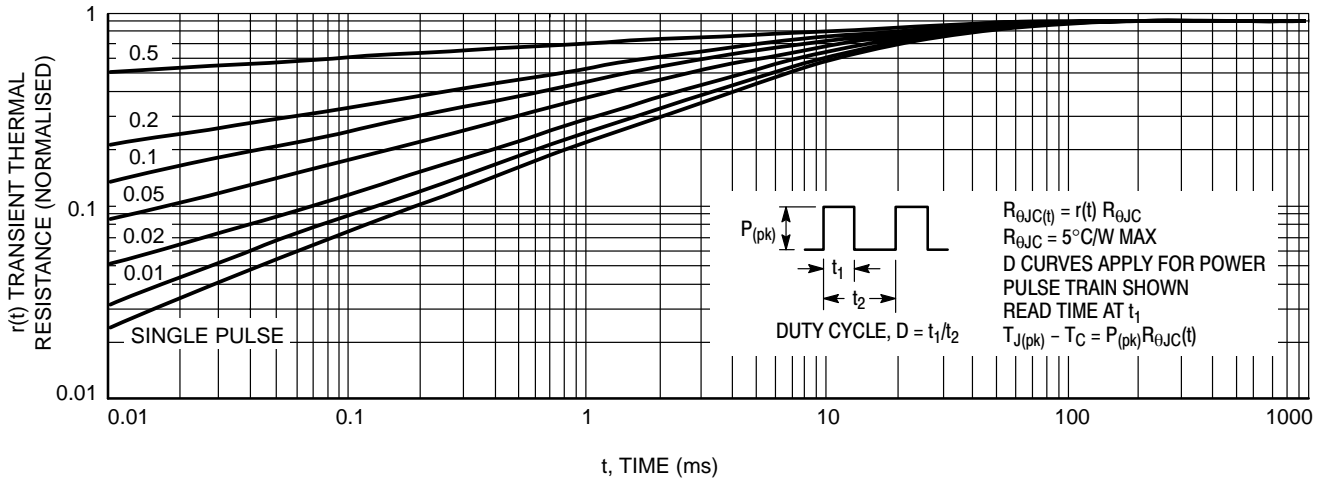


Figure 30. Typical Thermal Response ($Z_{\theta JC}(t)$) for MJD18002D2

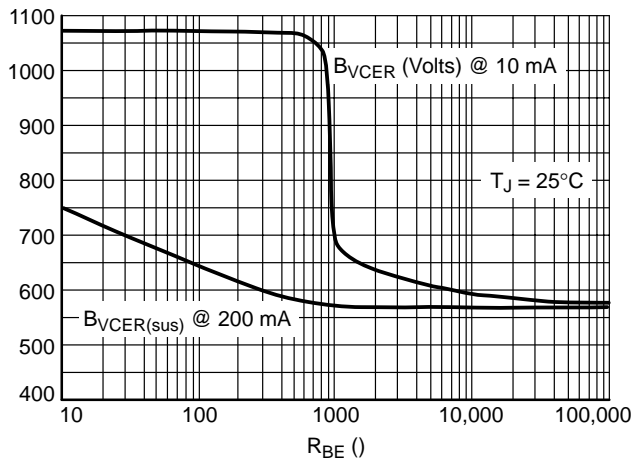


Figure 31. B_{VCER}

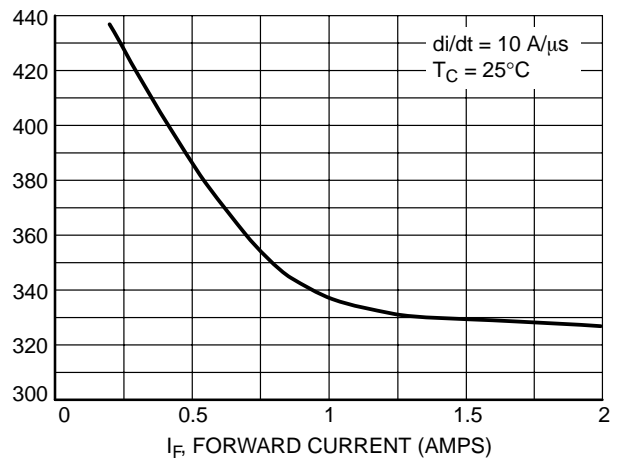


Figure 32. Forward Recovery Time, t_{fr}

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 33 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time.

The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

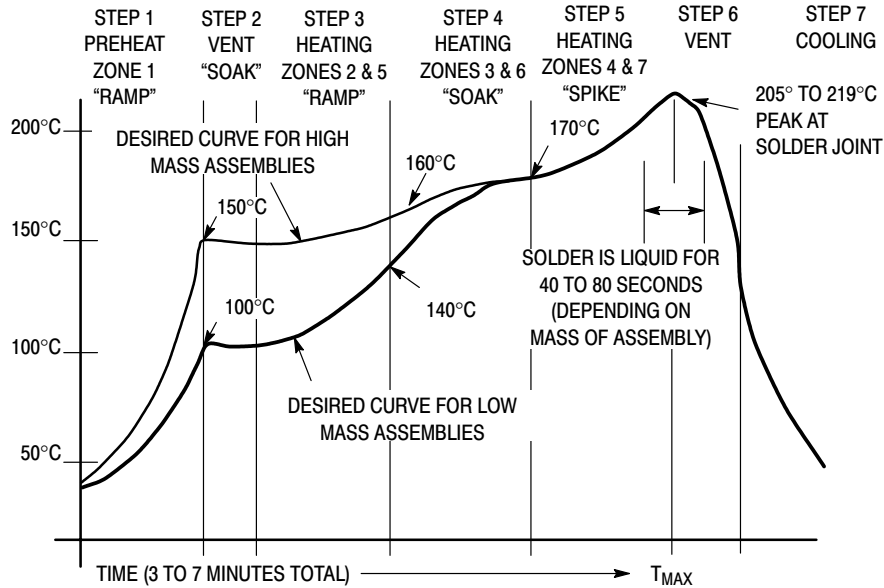
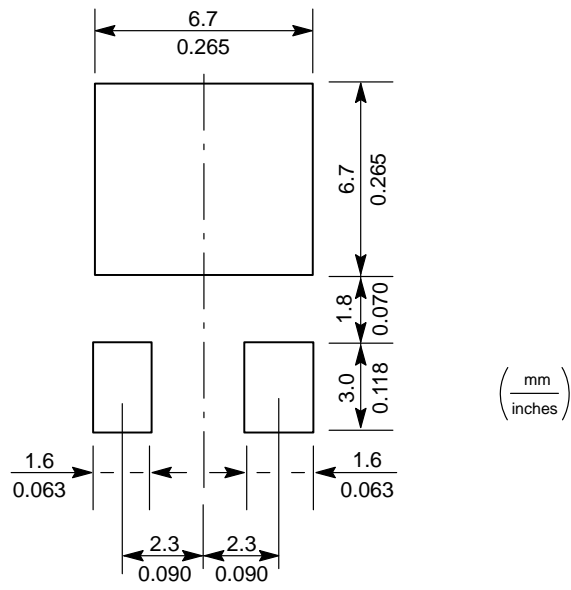


Figure 33. Typical Solder Heating Profile

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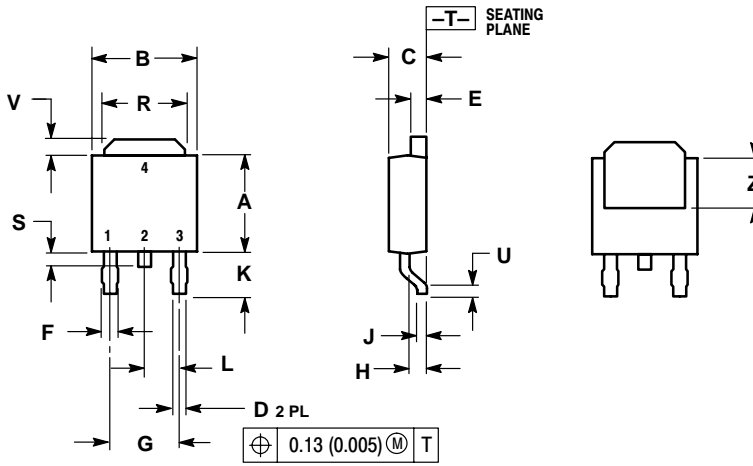
Minimum Pad Sizes Recommended for Surface Mounted Applications



MJD18002D2

PACKAGE DIMENSIONS

DPAK
CASE 369A-13
ISSUE AA



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	---	0.51	---
V	0.030	0.050	0.77	1.27
Z	0.138	---	3.51	---

STYLE 1:

- PIN 1. BASE
- COLLECTOR
- EMITTER
- COLLECTOR

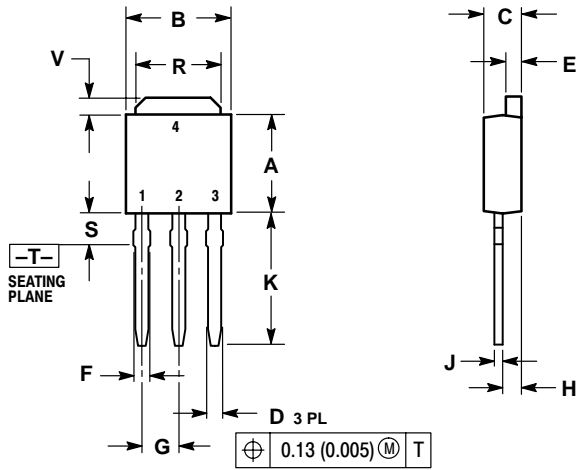
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PACKAGE DIMENSIONS

DPAK STRAIGHT LEADS

CASE 369-07

ISSUE M



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.175	0.215	4.45	5.46
S	0.050	0.090	1.27	2.28
V	0.030	0.050	0.77	1.27

STYLE 1:

- PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

Notes

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